Show your work and/or explain your answers. 110 points possible. Graded on 100 points.

1) a) (7 pts) You have an aluminum enclosure that attenuates a 30MHz external signal by 40db (a factor of 100). How much thicker would the enclosure have to be to attenuate the signal by another 20db (another factor of 10)? Give your answer as a percentage of the original thickness (Ex: 20% thicker).

The attenuation decreases by 1/e (8.7db) for every skin depth ($\delta$).

$20\text{db}/8.7\text{db} = 2.3\delta$, $40\text{db}/8.7\text{db} = 4.6\delta$, $60\text{db}/8.7\text{db} = 6.9\delta$

Increasing the thickness by 50% ($2.3\delta$) will increase the attenuation by 20db (a factor of 10).

b) (5 pts) You need to drill a hole in the above enclosure to run wires. What is the largest diameter hole you can drill and still maintain the original 40db shielding at 30MHz?

Shielding depends on $\lambda$. $\lambda = V/f = (3E8 \text{ m/s})/(3E7 \text{ Hz}) = 10\text{ m}$. 
$\lambda/2 = 1:1$ 0db, $\lambda/20 = 1:10$ 20db, $\lambda/200 = 1:100$ 40db attenuation

Therefore for 40db, $10\text{m}/200 = 0.05\text{m} = 5\text{cm}$

The diameter of the hole should be $\leq 5\text{cm}$ to maintain 40db shielding.

2) A 15V pulse is traveling down a 50Ω coax cable. If the cable were properly terminated the voltage across the terminator would be 15V.

a) (4 pts) What is the voltage across the terminator when the pulse reaches the end of the cable if $R = 25$ ohms?

$\Gamma = (Z_L-Z_S)/(Z_L+Z_S) = (25\Omega-50\Omega)/(25\Omega+50\Omega) = -1/3$

$15*(-1/3) = -5V$ is reflected back down the line

Therefore, 15V moving right, -5V moving left = 10V across the 25Ω terminator.

b) (4 pts) What is the voltage across the terminator when the pulse reaches the end of the cable if $R = 75$ ohms?

$\Gamma = (Z_L-Z_S)/(Z_L+Z_S) = (75\Omega-50\Omega)/(75\Omega+50\Omega) = 1/5$

$15*(1/5) = 3V$ is reflected back down the line

Therefore, 15V moving right, 3V moving left = 18V across the 75Ω terminator.

3) (6 pts) Fill out the truth table for this logic circuit.

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Page 1 (26 pts)
4) (8 pts) **Simplify** and implement this truth table with minimum number of gates.

![Truth Table and Logic Diagram]

5) a) (16 pts) Design an audio amplifier using a single op-amp. It should have **gain of 10** in the pass band (20Hz-20KHz) and drop off below 20Hz and above 20KHz. There are no input impedance requirements. **Label all parts.** Use the following:

   - LM741: 1MHz gain bandwidth product
   - +/-15V power supplies (add decoupling caps)

   \[ F_c = \frac{1}{2\pi RC} \]

   Gain = 100K/10K = 10 (20db)
   Fc (0.8uf & 10K) is 20Hz,
   Fc (80pf & 100K) is 20KHz

   Note: You could also use a non-inverting amplifier.

   ![Audio Amplifier Circuit Diagram]

b) (4 Pts) If you were to redesign the circuit for a higher gain (still using only one op-amp), estimate the max gain possible before limiting the pass band. Give a one-sentence explanation.

   The gain bandwidth product is 1MHz
   The bandwidth is 20KHz
   1MHz/20KHz = 50
   A gain of 50 is the best one can do with a single op-amp with a GBW of 1MHz.
6) Design a photodiode amplifier using the photodiode specified below and a single (ideal) op-amp. The amplifier should have a gain of +1V/uA (i.e. positive output) and have as little DC offset as possible.

a) (8 pts) Draw the complete schematic. Include power connections and decoupling caps. Use a +/-15V power supply.

Photodiode Specs:
I_{dark} = 10nA@15V reverse bias (at 25C)
Junction Capacitance = 100pf@0V reverse bias
Junction Capacitance = 10pf@15V reverse bias

To minimize DC offset the voltage across the photodiode should be 0V so there is no dark current.

Use a 1MΩ feedback resistor so the output is:
1uA*1MΩ = +1V/uA

b) (7 pts) If DC offset didn’t matter, how could the above single op-amp amplifier be sped up (redraw the schematic)? About how fast would it respond? Give a 1-2 sentence explanation.

By reverse biasing the photodiode with -15V its capacitance drops by a factor of 10. The RC time constant is 1MΩ*10pF.

\[ Fc = \frac{1}{2\pi RC} = 16KHz \]
7) (12 pts) Design a circuit using the 74HC123 that will trigger on the rising edge of an input pulse, wait 10us, and provide a 30us output pulse as shown in the timing diagram. Tie all unused inputs high or low and add a decoupling cap on the power supply. Label the input and output. You can assume the pulse width is equal to the RC time constant of the external R & C.

Looking at the timing diagram one needs to trigger on the rising edge of the input pulse so the input should go to B1. A1 should be low and CLR1 should be high to allow the AND gate to change when the input pulse goes high.

The Q1 should go to A2 to trigger on the falling edge of Q1. This time B2 and CLR2 should be high to allow the AND gate to change when the input pulse goes low.

10K*1nf = 10us
30K*1nf = 30us

8) (6 pts) Fill out the timing diagram for A, B, & C. Note: The initial states of the flip-flop are shown in the timing diagram. The flip-flop clocks in data on the rising edge of the clock.

The initial conditions for ABC are 110. Note: The input to the first flip flop is A AND C NOT which is 1. A one gets clocked into the first flip-flop and A, B, & C shift one to the right.

On the remaining clock cycles the output of the AND gate is 0.
9) a) (4 pts) Complete the power supply schematic by adding a transformer and bridge rectifier to the 5V regulator.

![Schematic Diagram]

b) (4 pts) What is the minimum value for C (the filter capacitor) to limit the ripple voltage to 1V for the load shown?

\[
\Delta V_{\text{cap}} \text{ for constant } I \quad \Delta V = \frac{I \Delta T}{C}
\]

\[
C = \frac{1A}{1V \times 120 \text{ sec}} = 8,333uF
\]

C > 8,333uF to limit the ripple to <1V with a 1A load.

c) (4 pts) Write the minimum voltages at each point on the schematic above. Calculate the minimum RMS voltage rating for the transformer to ensure the regulator works properly and write it below.

The voltage regulator requires 2V of headroom so the input shouldn’t drop below 7V.
Allowing for 1V of ripple the regulator input will range from 7-8V.
The bridge rectifier will drop about 1.5V (two diodes active at a time).
7V + 1V ripple + 1.5V diodes = 9.5V DC
9.5V
\[
\frac{V}{\sqrt{2}} = 6.7V \text{ AC}
\]
The transformer should be rated at more than 6.7VAC to guarantee the regulator works with a 1A load.

d) (4 pts) If the regulator’s thermal resistance is 5C/W and it’s properly attached to a 25C/W heatsink, how far above the ambient temperature would the regulator die if operated with the load shown? Assume the input to the regulator is 8V.

5C + 25C = 30C/W, Power = V*I = (8V-5V)*1A = 3W, 3W*30C/W = 90C above ambient
10 (7 pts) Design a relay driver using the FET or BJT used in class. There is a 12V (up to 100mA) power supply available. When a 5V (up to 10mA) control line goes high the relay should come on. When the control line goes low or is disconnected the relay should go off. The relay, BJT, and FET specs are shown below. Label all component values on the schematic and show your calculations.

N channel FET: IRL2910 (see graph), Vds_max = 100V, Rds_on = 0.26 ohms

NPN transistor: 2N3904 with Hfe = 100, Vce_max = 40V, Ic_max = 200mA

Relay coil: 12V@50mA

Transistor:  
Hfe = 100 so base current ~0.5mA.  
Add a factor of 3 for a safety margin (1.5mA).  
Rb = (5V-0.7V)/1.5ma = 2.87K.  
Use 2.47K for safety.  
The diode clamps the HV kickback from the relay inductance when turned off.

FET: From the graph we can see that a gate voltage of >2.5V is sufficient to turn on the FET for a load of 50mA and at 5V the FET is almost fully on. We’re told that the relay should go off if the control signal is disconnected. A resistor will be added from gate to ground to drain the charge on the gate when not being driven.