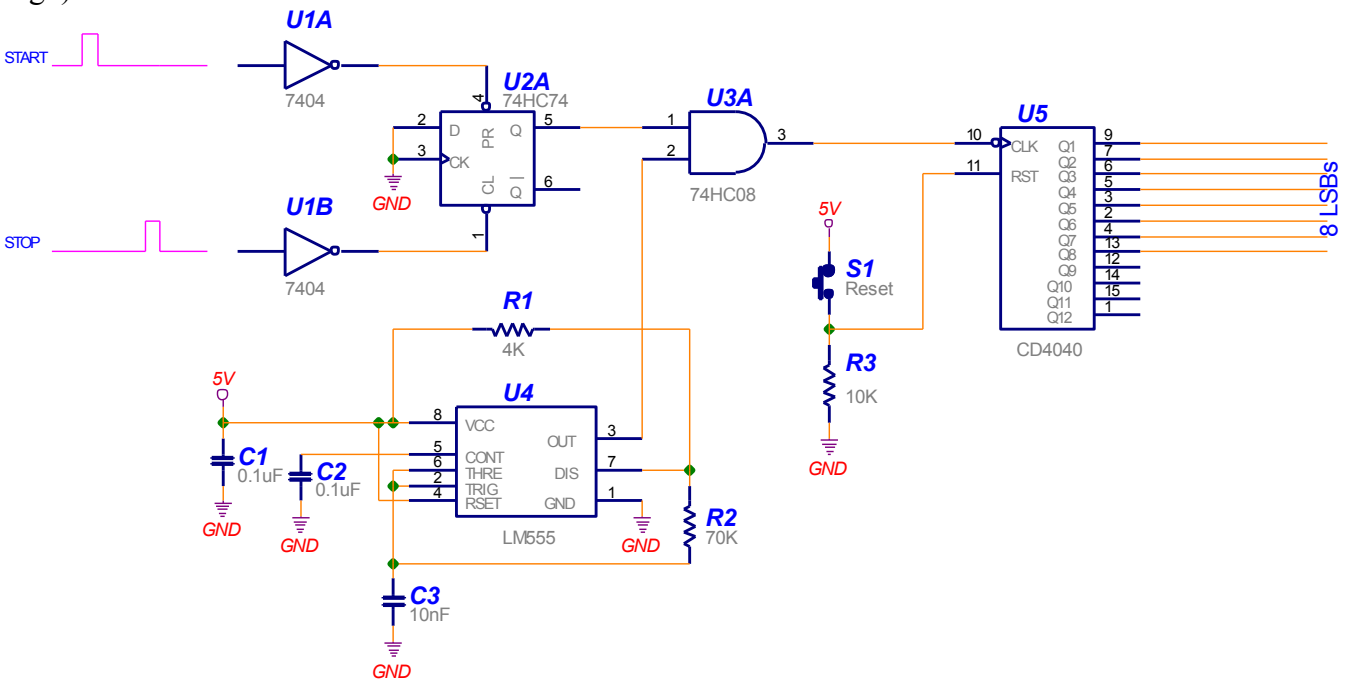
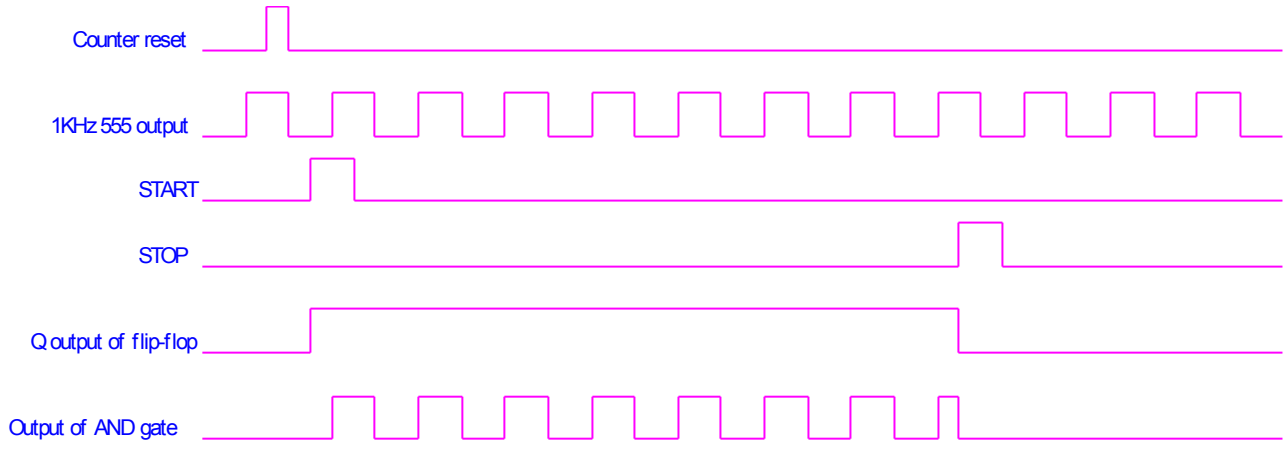
Homework #10 Solution

Since the preset and clear lines on the flip-flop are active low you need to invert the start and stop pulses since they're active high. In class we used a resistor to tie these lines high and brought them low by grounding the inputs. The Q output of the flip-flop will go high when the start pulse comes in and go low when the stop pulse comes in. The flip flop output is used to gate the clock to the counter on and off with an AND gate. The 555 timer is configured as an oscillator and the resistors and capacitor are chosen to oscillates at 1Khz. The counter is reset when the switch is pressed (the reset on the 4040 counter is active high).



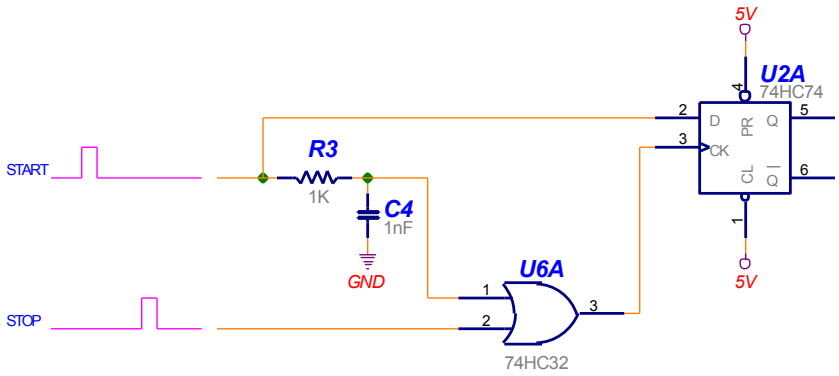
The timing diagram is shown below. The counter is reset, the start pulse comes in, the Q output of the flip-flop goes high, the counter starts counting, the stop pulse comes in, the Q output of the flip-flop goes low and the counter stops counting. The counter now has a count (1ms per count) representing the time between the start and stop pulses.



Binary output would be 00001000 (a count of 8, counts on falling edge)

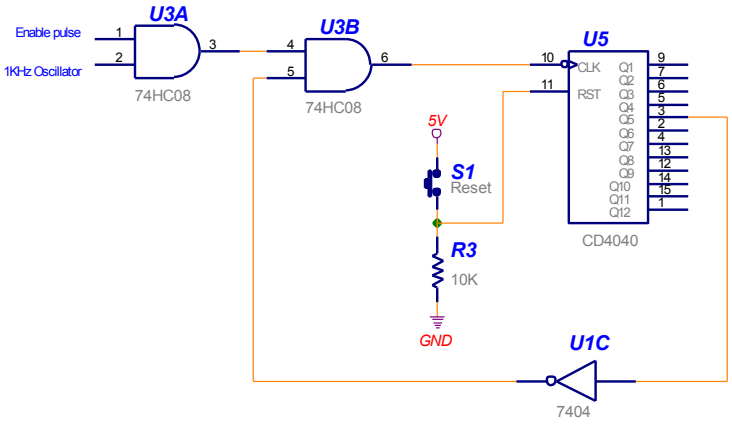
We could also build the circuit without the inverters (shown below):

By tying the preset and clear to 5V we can use the flip-flop as a flip-flop (i.e. when the clock goes high the D input gets transferred to the Q output). The RC filter has a time constant of 1us so the output of the RC filter will follow the input but be delayed by about 1us. This makes sure that the start pulse reaches the D input before the clock goes high.



Summary:
Both the start and stop pulses cause the clock on the flip-flop to pulse high. Only when the start pulse comes in will there be a one present at the D input and therefore only when the start pulse comes in will the output of the flip-flop go high. When the stop pulse comes in the flip-flop will clock in a zero (i.e. the D input is low) and the output of the flip-flop will go low. The output of the flip-flop can be used to gate the clock on and off as in the previous circuit.

If you want to stop the counter when the count reaches 16 you could do it like this. When the counter is reset all the outputs are low therefore the output of the inverter gate will be high (enabling the clock to the counter and the circuit will work as before). When the counter reaches 16, Q5 will go high, the output of the inverter will go low and the AND gate will disable the clock to the counter leaving the count at 16.



Instead of stopping the clock if you wanted an output to go high at a specific count you could do it like this. Only when Q1, Q2, Q6, & Q7 are high and Q3, Q4, Q5 & Q8 are low will the output of the final AND gate will be high. Replace the counter with a serial input, parallel output shift register and you have a digital lock that will only open when the proper code is entered.