PHYS 483/683 Final Exam 12/10/07 Name:________________________________

1) You want to shield a circuit from a nearby transmitter by putting the circuit in an aluminum enclosure. The transmitter is transmitting at 10.89 MHz and the skin depth of Aluminum (in inches) is $3.3/\sqrt{f}$.

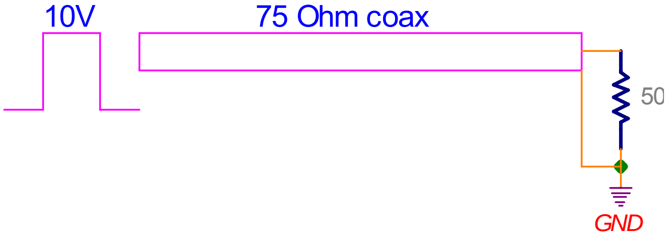
a) (5 pts) How thick would the enclosure have to be to attenuate the 10.89 MHz signal by 40db (i.e. a factor of 100)?

The skin depth is $3.3/\sqrt{10.89MHz}$ = 0.001 inches. The field gets attenuated by 1/e for every skin depth of thickness. Therefore the enclosure would need to be ln(100) = 4.6 skin depth thick (0.0046 inches).

b) (5 pts) How big of a hole can there be in the enclosure and still have 40db attenuation at 10.89 MHz?

You know that if the largest dimension of the hole is 1/20λ the signal will be attenuated by a factor of 10. If the hole is smaller than 1/200λ the signal will be attenuated by at least 100.
λ = (3E8m/s)/(10.89MHz) = 27.55m. 1/200λ = 13.8cm.

2). A 10V pulse is traveling down a 75Ω coax cable that is terminated with a 50Ω resistor.



a) (5 pts) What is the voltage across the terminator when the pulse reaches the end of the cable?

Reflection Coef = (50Ω-75Ω)/(50Ω+75Ω) = -0.2. 20% of the pulse is reflected back with the opposite polarity. 10V – 2V = 8V across the 50Ω resistor.

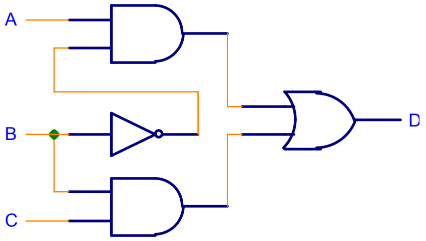
b) (5 pts) If the 50Ω resistor is replaced with a 100Ω resistor what is the voltage across the terminator when the pulse reaches the end of the cable?

Reflection Coef = (100Ω-75Ω)/(100Ω+75Ω) = +0.143. 14.3% of the pulse is reflected back with the same polarity. 10V + 1.43V = 11.43V across the 100Ω resistor.

Note: it's OK to have more voltage across a larger terminating resistor, energy is conserved.
Power = V^2/R
Initial = $(10V)^2/75\Omega$ = 1.333W
Resistor = $(11.43V)^2/100\Omega$ = 1.306W
Reflected pulse = $(1.43V)^2/75\Omega$ = 0.0273W
Initial energy = energy dissipated in resistor + energy reflected

3) (5 pts) Fill out the truth table for this logic circuit.

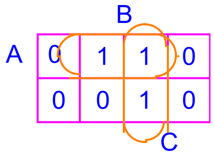
This is a multiplexer (MUX). When B is high C goes through to the output. When B is low A goes through to the output.

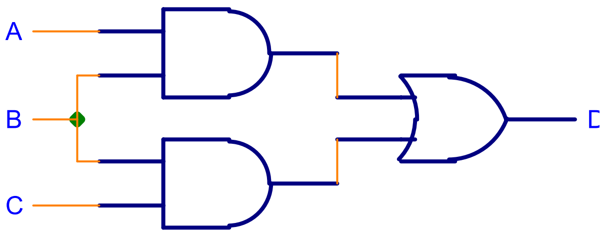


A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

4) (7 pts) **Simplify** and implement this truth table with logic gates.

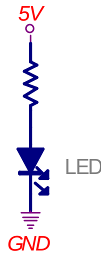
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1





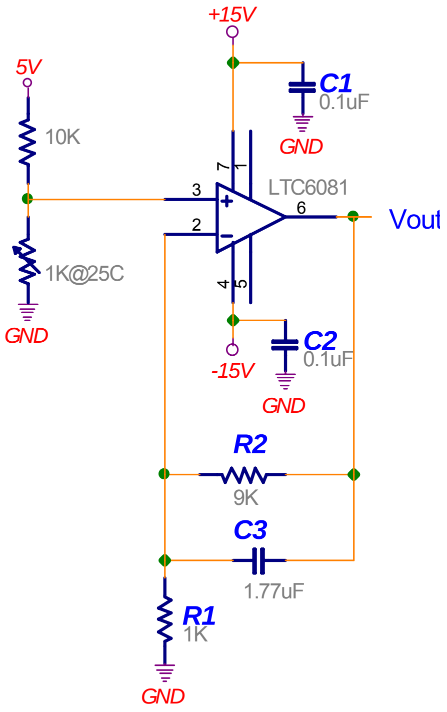
The Karnaugh map shows that the truth table can be simplified to AB + BC

5) (3 pts) What value should the resistor be to put 10mA through the LED? Note: the LED has a forward voltage drop of 2V@10mA.



If the LED drops 2V@10mAthat leaves 3V across the resistor. 3V/10mA = 300Ω.

6) (15 pts) a) Design an amplifier to amplify the output of the thermistor temperature sensor shown below by a factor of 10. The gain should roll off for frequencies above 10Hz (Note: the gain **doesn't** have to go all the way to zero at high frequency).



The non-inverting amplifier is used because of its high input impedance. The source (i.e. the thermistor) is a 1KΩ resistor so the input impedance of the amplifier should be much higher than 1KΩ.

The gain in the pass band is 1 + R2/R1 = 1+9 = 10. R1 & R3 were chosen to be 1KΩ & 9KΩ. C3 is chosen to roll off the gain at frequencies above 10Hz. 1/(2πR2C3) = 10Hz, therefore C3 = 1.77uF.

Note: If you were building this amplifier you would probably use a 0.1uF capacitor (17.7 times smaller and non-polarized) and multiply R1 & R2 by 17.7 (R1 = 17.7KΩ & R2 = 159.3KΩ). Usually the corner frequency doesn't need to be exactly 10Hz. Resistors come in many sizes, capacitors, not so many.

b) (5 pts) Which of these op-amps would be best for the above design and why

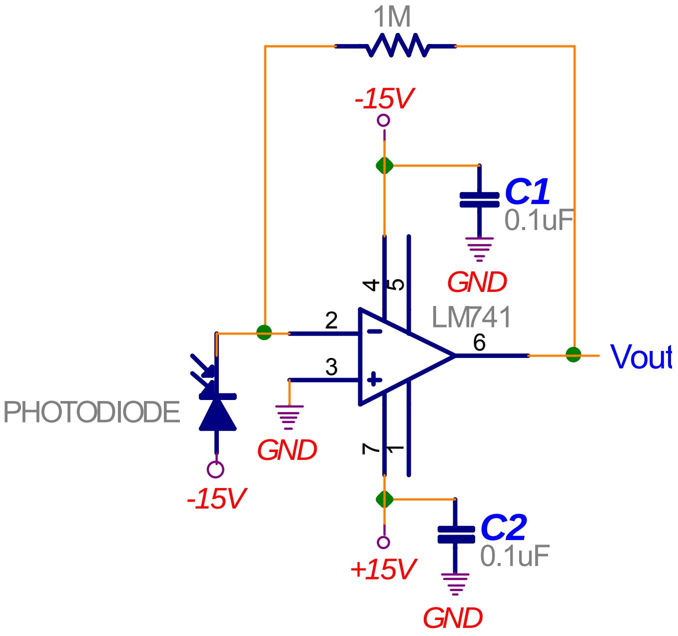
op-amp	Input Offset Voltage	Gain Bandwidth Product
LTC6081	70μV	3MHz
LT1210	15mv	35MHz

The LTC6081 would be better because it has a much lower Input Offset Voltage (the DC error will be less with this amplifier). The lower bandwidth also means less noise since we're amplifying slow moving signals (near DC).

7) Design a photodiode amplifier using the photodiode specified below and an op-amp (you can assume the op-amp is ideal). The amplifier should have an output of **+1V** when 1uW of light hits the photodiode (i.e. 1V/1uW). The light is passed through a beam chopper before hitting the photodiode. The light is chopped 1000 times a second so the amplifier should be able to respond to a 1KHz input.

a) (15 pts) Draw the complete schematic. Include power connections and decoupling caps (use any power supply you need).

Photodiode Specs:
I_{dark} = 1nA
Sensitivity = 1uA/uW
Junction Capacitance = 2nf@0V reverse bias
Junction Capacitance = 100pf@15V reverse bias



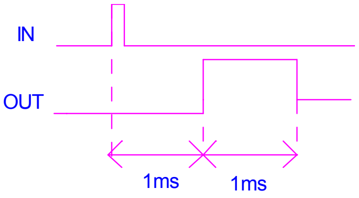
Use a current to voltage converter to convert the photodiode current to a voltage. The photodiode polarity must be as shown to get a positive output when light hits the photodiode. The 1MΩ feedback resistor gives us the 1V/uA required.

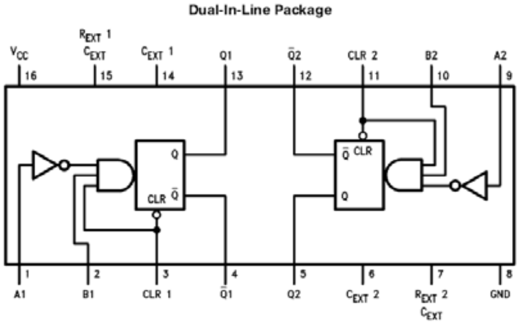
The response time of the amplifier is about the same as the RC time constant. With no reverse bias the response time is 1MΩ*2nf = 2ms (too slow to handle a 1KHz input). With a 15V reverse bias the response time is 1MΩ*100pf = 0.1ms. This is just fast enough to handle a 1KHz input.

b) (5 pts) What is the output voltage of your amplifier when no light is hitting the photodiode?

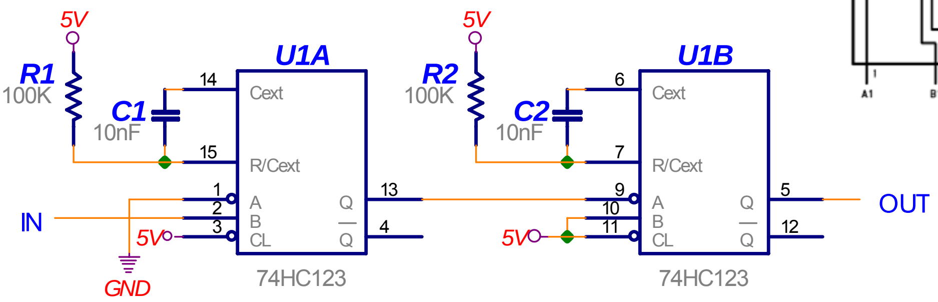
When no light hits the photodiode the only current it generates is the dark current (1nA). The output voltage is therefore 1nA*1MΩ = 1mV.

8) (15 pts) Design a circuit using the 74HC123 that will trigger on the rising edge of an input pulse, wait 1ms, then provide a 1ms output pulse. Tie all unused inputs high or low. Label the input and output. You can assume the pulse width is equal to the RC time constant of the external R & C.

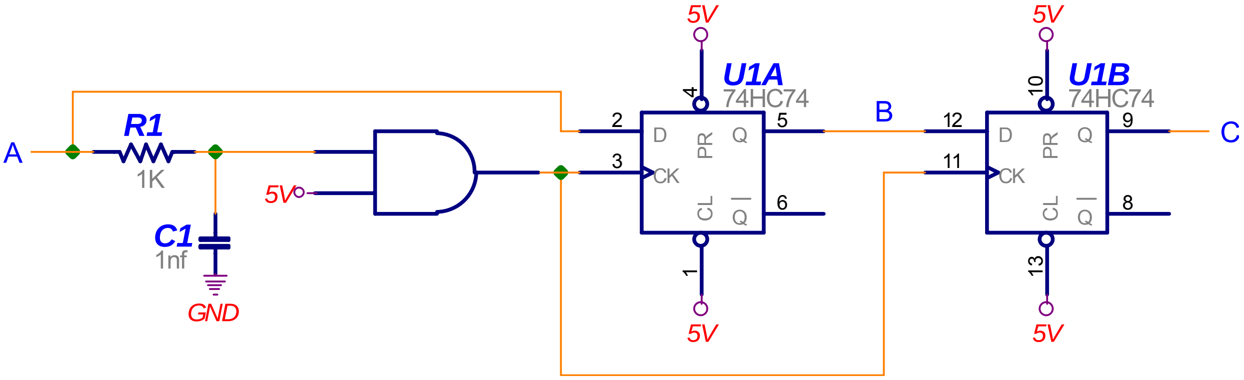




R1C1 & R2C2 are chosen such that the time constant is 1ms. The B input (pin 2) triggers on the rising edge. The output of U1A (pin 13) lasts for 1ms. When it goes low it triggers the A input of U1B. The output pulse (pin 5) lasts 1ms.



9) (10 pts) Fill out the timing diagram for B & C. Note: B & C are initially low. The 74HC74 clocks in data on the rising edge of the clock. You can assume A is clean 1Hz square wave and the AND gate has schmitt trigger inputs.



This is similar to the digital lock circuit you built. R1 & C1 delay the clock signal so that A arrives at the input to the flip-flop about 1us before the clock pulse. The schmitt trigger AND gate cleans up the slower moving input. Therefore whenever A goes high a one is clocked into the first flip-flop. The second flip-flop gets the output of the first flip-flop (just like the shift register).