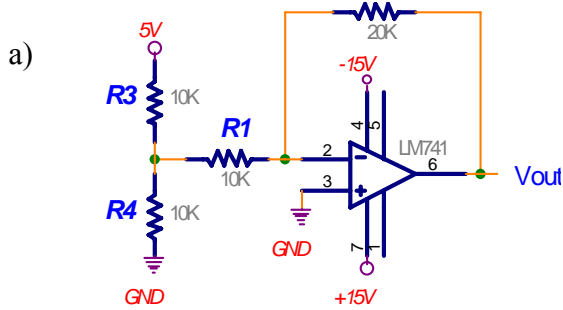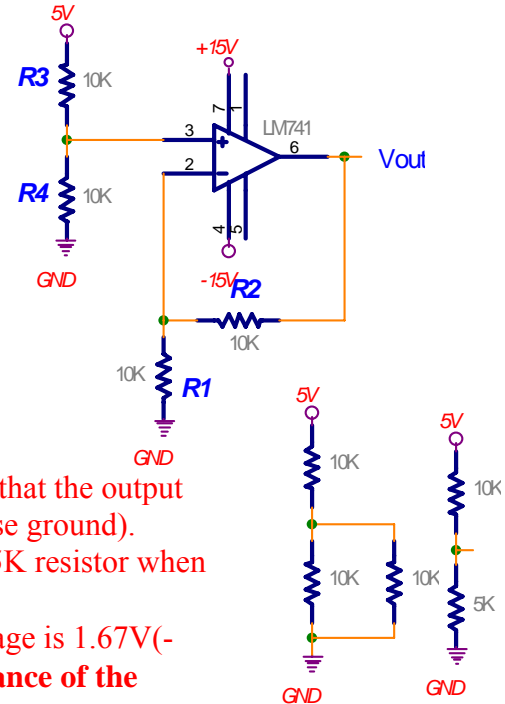1) What is the output voltage of the following two circuits?

a)

b)

a) The input impedance of the inverting amplifier is R1.  Recall that the output voltage adjusts to bring V- to the same voltage as V+ (in this case ground). Therefore R4 and R1 are in parallel and can be replaced with a 5K resistor when figuring out the voltage at the input.   The voltage at the input is 5V(5KΩ/15KΩ)=1.67V.  The gain is –R2/R1 so the output voltage is 1.67V(-20KΩ/10KΩ)= **-3.33V.  This is a case where the input impedance of the amplifier is too low for the circuit and affects the results.**

b) The input impedance of the ideal non-inverting amplifier is infinity.  Therefore the voltage at V+ is 2.5V.  The gain is 1+R2/R1 = 2.  The output voltage is therefore 2.5V(2)= 5V.

2) Design a single op-amp amplifier with the following frequency response.  Draw a complete schematic including power connections and decoupling caps.  Show calculations for the cutoff frequency and gain. You can use any power supply.

There weren't any requirements given for the input impedance so it's OK to use an inverting amplifier. If we pick R1 = 10KΩ and R2 = 100KΩ that will give us a gain of 10.  Actually the gain is –10 but for an audio amplifier inverting the signal doesn't matter.  The gain graph above also specifies the absolute value of the gain to be 10.  I forgot to show the rate at which the gain decreases.  We'll assume its 20db/decade (i.e. a single pole filter).  The corner frequency is 1/(2πRC).  For a 100hz and 10KΩ we get 0.16uF. For 10Khz and 100KΩ we get 160pf.  Note:  The gain bandwidth product of the 741 is 1Mhz and our gain is 10@10Khz so the op-amp is fast enough for our needs.  I also left of the power supply decoupling caps for clarity.  Ideally you would have 0.1uf or so from each power rail to ground.
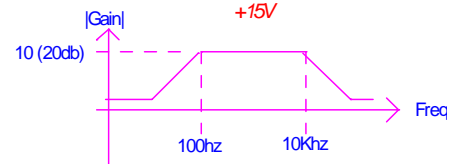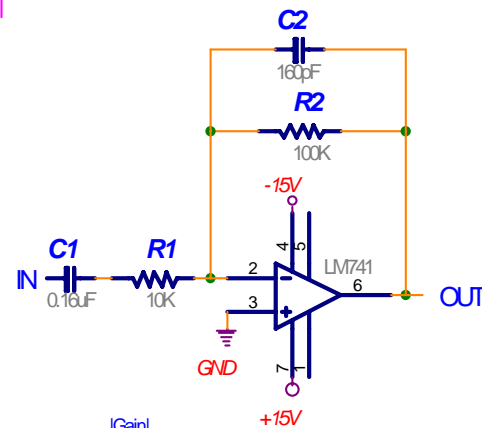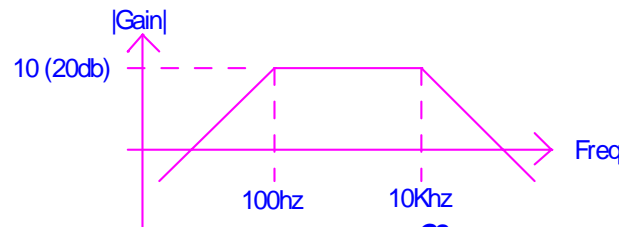
Note: If a non-inverting amplifier was used the gain wouldn't decrease below 1 since the gain is 1+R2/R1 (see the frequency response graph to the right).

3) Given the following three op-amp choices, which op-amp would be the best choice if the main requirement is to design an:

| Op-Amp | Input Off-Set Voltage (mv) | Gain Bandwidth Product (Mhz) |
| --- | --- | --- |
| A | 0.1 | 1 |
| B | 1 | 20 |
| C | 3 | 1 |

a) Audio amplifier with a gain of 100 from 20hz-20Khz.

Need a gain bandwidth product of at least 100*20Khz = 2Mhz so the only op-amp fast enough is **B**.

b) Thermocouple amplifier where Vin is a few mV.

A thermocouple amplifier is amplifying small (few mV size) signals and low speed (less than 1hz). The op-amp with the lowest input off-set voltage is desirable. Therefore **A** is the correct choice.

4) You are asked to design a circuit to count objects on an assembly line. There is already an LED mounted on one side of the conveyor belt and a matching photodiode on the other. As objects move past the light beam is broken. They have a digital counter (with a schmitt trigger input) that will register a count whenever the input is greater than 3V (the counter can handle input voltages up to 15V without damage).

LED specs:
2V forward drop
Imax = 20mA
Efficiency = 0.1mw/mA

Photodiode Specs:
Idark = 1nA
Sensitivity = 1A/W
Capacitance = 1nF@0V reverse bias (0.1nF@15V reverse bias).

a) Design a circuit that will drive the LED and amplify the photodiode signal such that it will count when the light beam is blocked. You can assume that 100% of the light leaving the led hits the photodiode (lenses are used). Draw a complete schematic including power and decoupling caps. Use any power supply you want.

We'll use a current to voltage converter to convert the output current from the photodiode to a voltage for the counter. The photodiode polarity is such that the output voltage will be positive since we need a voltage above 3V to be a legal count. Since the max input voltage on the counter is +15V we'll use +/- 15V power supplies since the output of the op-amp can't go above 13.5V (within about 1.5V of either power rail). We also need the output voltage when no light is hitting the diode to be less than 3V (depends on the dark current).

Let's start with the LED. Since it has a max current of 20mA lets operate it at 10mA and see if we can make it work. At 10mA the LED puts out 10mA(0.1mw/mA) = 1mw. We're told that all of this light hits the photodiode. The photodiode has a sensitivity of 1A/w so we should get 1mA of current from the photodiode when the light isn't being blocked.
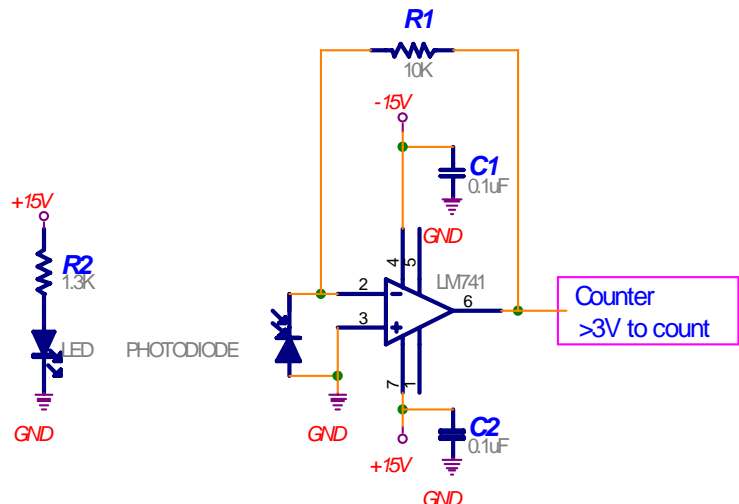
If we use a 1KΩ feedback resistor this would give us a 1V output.  We need >3V.  Lets us a 10KΩ.  This will give us a 10V output when light is hitting the photodiode. The dark current is 1nA so with no light the output voltage will be 1nA*10KΩ = 10uV (small enough we can ignore).

b) About how fast can your circuit respond with no reverse bias?

The response time is usually limited by the RC time constant R1*$C_{diode}$ (10KΩ*1nF = 10us).  In this case the LM741 is a very slow op-amp with a typical slew rate of 0.5V/us (meaning in 10us the output voltage could only change by about 5V).  So in this case the op-amp is limiting the response time.

c) What is the maximum count rate for your circuit with a 15V reverse bias?

With a 15V reverse bias the diode capacitance is 10 times smaller (0.1nf).  With a faster op-amp the maximum count rate would be 10 times faster than before.  But with the slow LM741 there is no benefit to reverse biasing the photodiode.
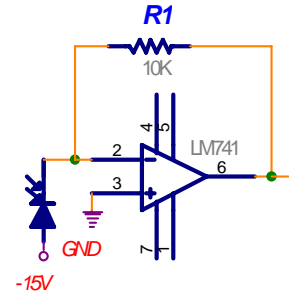
To figure the max count rate we now the counter has to get above 3V to be counted.  It wasn't specified what voltage is a legal low so let's make the output slew from 0V to 3V and back to 0V (one count).  That's a total swing of 6V.  With a slew rate of 0.5V/us it would take 12us.  Throw in a little safety margin and we'll say 15us per count or 66.7Khz (fast for an assembly line).

5) At t=0 the switch is closed.  At t = 5ns the switch is opened.  The propagations speed in the coax is 2E8m/s (1m/5ns).  The right side of the 50Ω cable isn't connected to anything.
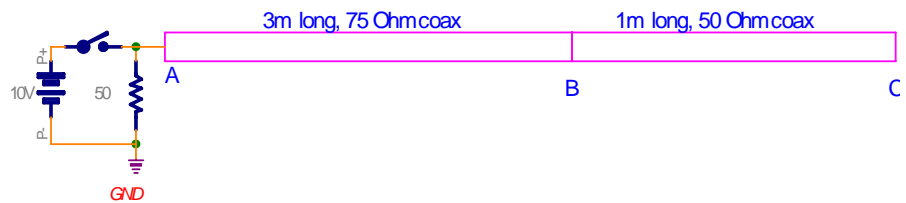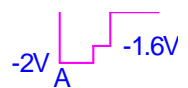
a) What is the voltage at B at t = 17ns?

At t = 15ns the pulse reaches B.  P of the pulse is reflected back towards A and part continues towards C.  The reflection coefficient is (50Ω-75Ω)/(50Ω+75Ω) = -1/5.  We start with a 10V pulse on the cable.  When it hits B 1/5 of the voltage is reflected back with the opposite polarity (10V-2V=8V on the 75Ω coax at B).  In the 75Ω coax the rest of the 10V pulse continues to move to the right and a –2V pulse is moving to the left).  4/5 of the 10V pulse continues to propagate towards C (8V on the 50Ω coax at B).
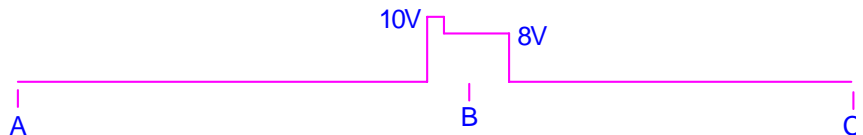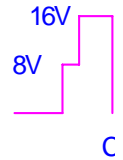
b) What is the voltage at A at t = 32ns?

The –2V pulse reaches A at 30ns.  Because the cable is improperly terminated (50Ω again instead of 75Ω) 1/5 of the signal will be reflected with the opposite polarity.  At 32ns the voltage a A is the sum of the –2V pulse going left and the +0.4V reflected pulse going right.   A is therefore -1.6V.

c) What is the voltage at C at t = 22ns?

The 8V pulse reaches C at 20ns. At 22ns the pulse has hit the open end of the cable and reflected back with the same polarity and magnitude. C is therefore 16V (the sum of the 8V pulse moving right and the 8V pulse moving left)

d) What is the voltage at A at t = 42ns?

At 25ns the 8V pulse moving left will hit B and 1/5 will be reflected back with the same polarity and 6/5 will continue on toward A with the same polarity (voltage must be continuous across the boundary).

This pulse is 8V(6/5) = 9.6V. When it hits the impedance mismatch (50Ω terminating resistor) 1/5 will reflect back with the opposite polarity and 4/5 will be absorbed by the 50Ω resistor. Therefore, the voltage at A at 42ns is 9.6V pulse going left and the -1.92V reflected pulse moving right (i.e. 9.6V – 1.92V = **7.68V**).
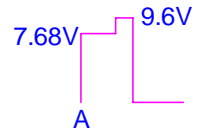
Note: It's OK for the voltage to increase when the pulse goes from the 50Ω cable into the 75Ω cable. Energy is conserved.
Power = $V^2/R$
Initial pulse = $(8V)^2/50Ω$ = 1.28W
Transmitted into 75Ω cable = $(9.6V)^2/75Ω$ = 1.2288W
Reflected pulse in 50Ω cable = $(1.6V)^2/50Ω$ = 0.0512W
Initial 50Ω (1.28W) = transmitted into 75Ω (1.2288W) + reflected back into 50Ω (0.0512W)

Note: The 0.4V pulse that reflected of A at 30ns is heading toward B and won't affect the voltage at A at 42ns. The pulses don't overlap at 42ns.

6) The skin depth of Aluminum (in inches) is $3.3/\sqrt{f}$.

a) How thick would an aluminum enclosure have to be to attenuate a 10Mhz signal by a factor of 10 (20db)?

$e^n$ = 10, n = ln(10) = 2.3, so to attenuate the signal by a factor of 10 the enclosure has to be at least 2.3 skin depths thick. The skin depth of Aluminum at 10Mhz is $3.3in/\sqrt{10Mhz}$ = 1.04 mils (1mil = 1/1000 of an inch). So the enclosure should be at least 2.3*1.04mils = 2.4 mils thick.

b) How large of a hole could there be in the enclosure and still attenuate a 10Mhz signal by a factor of 10 (20db)?

There is a factor of 10 attenuation when the largest dimension of the hole is 1/20λ. λ = 3E8/1E7 = 30m. 30m/20 = 1.5m. Note: if the hole is 0 times smaller the attenuation would be 10 times larger.
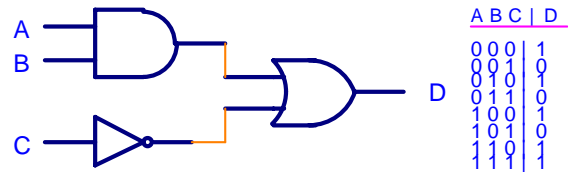
7) Which has a lower DC resistance, one 2mm diameter wire or two 1mm diameter wires?

The 2mm diameter wire has lower DC resistance because it has a larger cross sectional area than the two smaller wires combined.
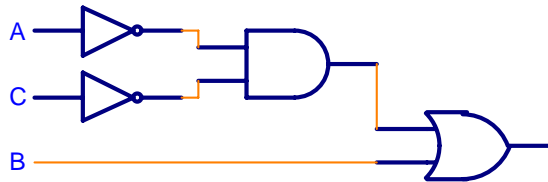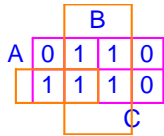
8) Which would have a lower AC resistance (say at 1Ghz)? The one 2mm diameter wire or two 1mm diameter wires (or does it matter)?

9) Fill out the truth table for the following logic circuit:

| A | B | C | D |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

10) Draw the simplest logic circuit that will implement the following truth table:

| A | B | C | D |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

|   | B |   |   |
|---|---|---|---|
| A | 0 | 1 | 1 | 0 |
|   | 1 | 1 | 1 | 0 |
|   |   | C |   |   |

11) When configured as an oscillator the frequency of the 555 timer is $f = \dfrac{1.44}{(R1 + 2R2)C}$. Draw the schematic of a 555 timer that will oscillate at 1Khz.

12) Configure a 74HC123 to provide a 50us pulse after a 50us delay when triggered by a falling edge on the input (see diagram below). Draw the schematic and label the input and output. You can assume the width of the pulse is equal to the RC time constant.

**Dual-In-Line Package**
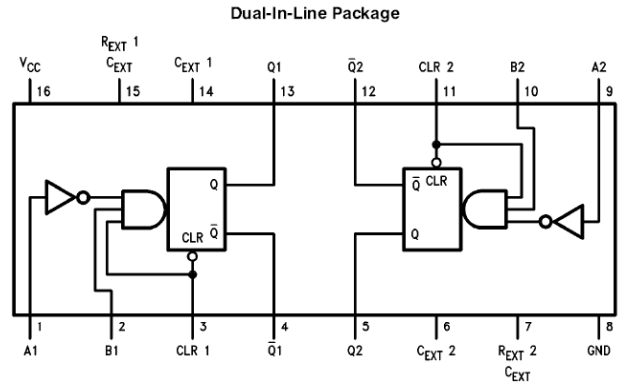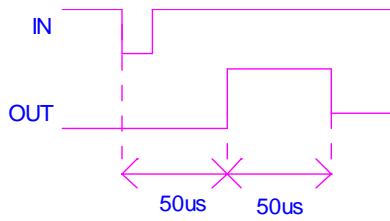


The clear line is active low (meaning it clears the output when low) so it's tied high (never leave unused inputs floating on CMOS parts). The input is sent into the A input since it triggers on the falling edge (note: the B input triggers on the rising edge). R1C1 & R2C2 = 50us. Pin 13 goes high the instant pin 1 goes low. Pin1 stays high for 50us (this is the delay). When pin 1 goes low it triggers U1B and pin 5 goes high for 50us (this is the output pulse).
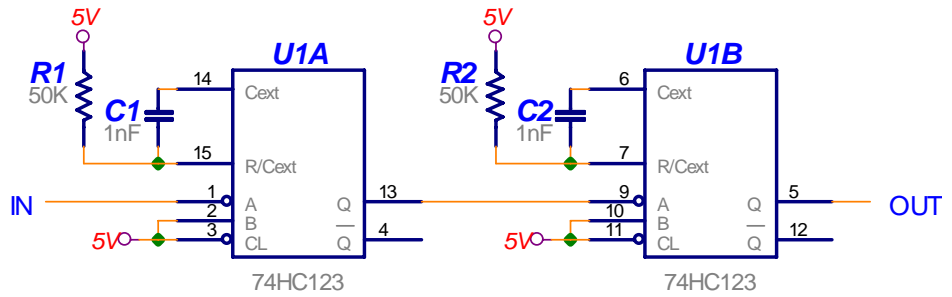
Alternately the inverted output (pin 4) could have been used to trigger the B input on U1B.
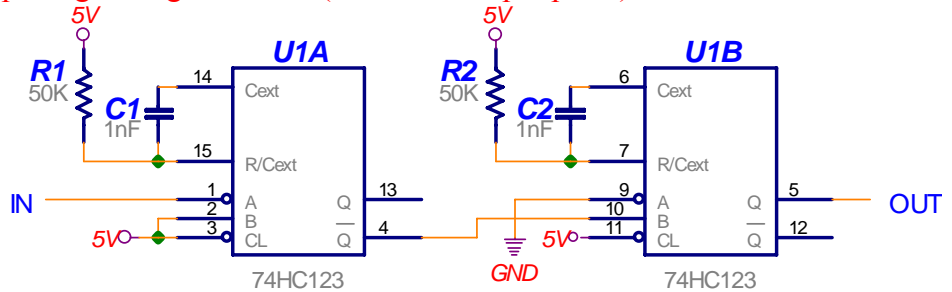
13) Fill out the timing diagram for C after t = 0. Note: C is high before t = 0.
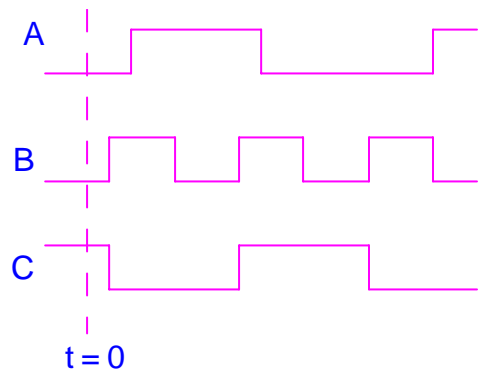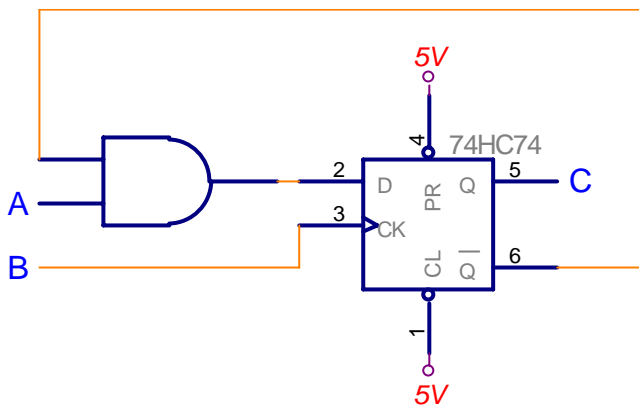


I forgot to say that the flip-flop is a 74HC74 and clocks the data in on the rising edge (for the test I'll tell you which clock edge to use). At t=0 C is high so pin 6 is low and therefore the output of the AND gate is low. When the first rising edge of the clock comes in a low is clocked into flip-flop (C goes low). The output can't change until the next rising edge of the clock. At that time A is high and pin 6 is high so a one is clocked into the flip-flop (C goes high). On the third rising edge of the clock A is low so a zero is clocked into the flip-flop (C goes low).